# MSCDN – MP1

Check and System Synchronising Relays

## Document Release History

This document is issue 2010/02. The list of revisions up to and including this issue is:
Pre release

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| 2010/02 | Document reformat due to rebrand |
| 27/08/2008 | R6 Figures renumbered. Figure 4 redrawn with 50N connections added. |
| 20/10/2005 | R5 Page footer, “MSCDM” corrected to “MSCDN”<br>Software number added. |
| 24/05/2005 | R4 Removed 2nd paragraph Sec. 2.0 - references to CT-X,. Added Fig.3 Application of 87/50 Inhibit DO Delay |
| 28/04/2005 | R3 References to CT-X and 87/50-X removed. Use of 87/50 Inhibit DO Delay described. |
| 28/02/2003 | R2 50-3 Added |
| 07/02/2003 | R1 Revision History Added |

## Software Revision History

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# 1 INTRODUCTION

The MSCDN-MP1 represents an integration of the protection elements required to provide a single box Main 1 protection unit for capacitor banks, these include Overall Differential protection, Capacitor Unbalance protection, and additional Phase Unbalance backup protection. Together with it's sister units MSCDN-MP2A and MP2B, this protection unit offers a complete solution for Main 1 and Main 2 protection of EHV capacitor banks.

The relay is based on Reyrolle's Modular II protection family, which offers the following features as standard :-

- User programmable Output Relays, Status Inputs and LED indication
- Waveform Recording
- Fault Recording
- Remote interrogation of the state of the relay logic and of the stored fault data.

These notes give guidance on the application of the relay and the protection elements integrated in it, reference may be made to the Commissioning Chapter, which provides detailed set-up instructions.

# 2 OVERALL DIFFERENTIAL PROTECTION

Transient stability under through fault conditions is a problem with many forms of differential protection due to variations in CT magnetising characteristics. As saturation is approached, the CT output current waveforms become increasingly distorted with a high percentage of 3rd and other higher odd harmonics. These problems can be overcome by either using biased differential protection, or more elegantly by the use of high impedance schemes. In the latter case the relay settings are calculated assuming one CT is completely saturated. Using this worst-case condition the voltage and current settings for the 87/50 Overall Differential protection can be precisely calculated with known stability margins. Intermediate condition's, where a CT is only partially saturated, increases the stability margin. This approach enables schemes to be engineered using CT's with relatively low knee point voltages.

## 2.1 High Impedance Differential Protection

The stability of a current balance scheme using a high impedance relay circuit depends upon the circuit voltage setting being greater than the maximum voltage which can appear across the relay under a given through fault condition. A setting resistor or resistors, and non-linear resistor per phase, complete the scheme and are mounted externally to the relay. The voltage level required for stability and the value of relay current calculated to provide the required primary fault setting determines the resistor value. Non linear resistors protect the CT's and relay from the excessively high voltages which may occur e.g. for high values of in-zone fault current, see Figure 1 – Basic Dual Element High Impedance Differential .

### 2.1.1 Determination of Stability

The stability of a current balance scheme using a high impedance relay circuit is based on the fact that for a given through fault condition, the maximum voltage that can occur across the relay circuit is determined by means of a simple calculation. If the setting voltage of the relay is made equal to or greater than this voltage, then the protection will be stable. In calculating the required setting voltage of the relay it is assumed that one current transformer is fully saturated and that the remaining CT's maintain their ratio. In this condition, the excitation impedance of the saturated CT is negligible and the resistance of the secondary winding, together with leads connecting the CT to the relay terminals, constitute the only burden in parallel with the relay as shown in figure 2. Thus the voltage across the relay is given by:

V = I x (X1 + Y1) for CT1 saturated
V = I x (X2 + Y2) for CT2 saturated

Where :-
X1 and X2 = the secondary winding resistances of the CT's.
Y1 and Y2 = the value of the pilot loop resistance between the relative CT and the relay circuit terminals.
I = the CT secondary current corresponding to the maximum steady state through fault current of the protected equipment.
V = the maximum voltage that can occur across the relay circuit under through fault conditions.

For stability, the voltage setting, Vs, of the relay must be made equal to or exceed, the highest value of V calculated above. Experience and extensive laboratory tests have proved that if this method of estimating the relay setting voltage is adopted, the stability of the protection will be very much greater than the value of I used in the calculation. This is because a CT is normally not continuously saturated and consequently any voltage generated by this CT will reduce the voltage appearing across the relay circuit. The relay is a low burden, current operated relay and the stability voltage setting is achieved by employing a series resistor of appropriate ohmic value (e.g. depending on the current setting chosen) and power dissipation rating.

### 2.1.2 Current Transformer Requirements

For high impedance schemes it is necessary to establish characteristics of the CT in accordance with Class ‘X’ to BS 3938 and that where the CT’s are specifically designed for this protection their overall size may be smaller than that required for an alternative current balance protection. The basic requirements are:

- All CT’s should, if possible have identical turns ratios.
- The knee point voltage of each CT, should be at least 2 x Vs.
- The knee point voltage is expressed as the voltage applied to the secondary circuit with the primary open circuit which when increased by 10% causes the magnetising current to increase by 50%.

### 2.1.3 Overvoltage Protection

The maximum primary fault current in the protected zone will cause high voltage spikes across the relay at instants of zero flux since a practical CT core enters saturation on each half-cycle for voltages of this magnitude. Thus it is necessary to suppress the voltage with a non-linear resistor in a shunt connection, which will pass the excess current as the voltage rises. The type of non-linear resistor required is chosen by its thermal rating.

### 2.1.4 Fault Setting

The fault setting of a current balance protection using a high impedance relay circuit can be calculated in the following manner.

Primary fault setting = N (I + I1 + I2 + I3 +Ish)

where :-

I = the relay operating current. I1, I2, I3 = the excitation currents of the CTs at the relay setting voltage.
N = the CT ratio.
Ish = other shunt circuits where provided e.g. non-linear resistor etc.

The fault setting of the protective scheme depends upon the protected equipment and the type of system earthing.

## 2.2 Setting Example

A Setting Example is included in Application Guide – High Impedance Circulating Current Protection Calculations ( Report No. 990/TR/7/1 )

## 2.3 Application of 87/50 Inhibit DO Delay

The 87/50 Elements are high speed elements and in certain scheme configurations e.g. the application of in-zone surge arrestors, may operate due to switching transients. When it is not possible to reach a suitable compromise of security and dependability by application of the elements’ setting and stabilising delay, then a particular element may be inhibited via external signal. A signal is applied to a status input (Aux I/P), via either one of the CB auxiliary contacts or a control signal. Using the STATUS INPUT MENU, this signal may be inverted to realise the optimum scheme security, based on the use of NO or NC energising contacts. The signal is then logically connected to the 87/50 Inhibit and a combination of Aux I/P Pickup Delay and 87/50 Inhibit DO Delay used to optimise the required blocking period. See Figure 2 – Application of 87/50 Inhibit DO Delay.

# 3 CAPACITOR UNBALANCE PROTECTION

Although the relay capacitor unbalance element may be applied to other arrangements, such as Star-connected, Split star-connected and Delta-connected capacitor banks, it has primarily been designed for use on capacitor banks incorporating a single phase bridge arrangement, as shown in Figure 3 - Simplified Single Phase Bridge Capacitor Bank

## 3.1 Principal Of Operation

Consider Figure 3 - Simplified Single Phase Bridge Capacitor Bank, which shows the protection current measuring points $I_{Ref}$ and $I_{Spill}$.

$I_{Ref}$ being the chosen reference current, in this case the capacitor current, but which may be any current, which varies in proportion to $I_{Spill}$.

$I_{Spill}$ is the current measured across the H-section of the capacitor bank.

Consider the equation below, for an un-faulted capacitor bank, any given $I_{Ref}$ will produce a proportional Spill Current $I_{Spill}$, such that the ratio of $I_{Spill}$ to $I_{Ref}$ is a constant i.e.

$$\overrightarrow{Ratio} = \frac{\overrightarrow{I_{Spill}}}{\overrightarrow{I_{\mathrm{Re}\,f}}} \qquad \textbf{Eq. 1}$$

At Nominal Operating Conditions i.e. Rated Voltage, the Nominal Values for $I_{Ref}$ and $I_{Spill}$ can be calculated. Using these values, $I_{RefNom}$ and $I_{SpillNom}$, which are entered as settings, then the NomRatio may be calculated from Eq. 1.

$$\overrightarrow{NomRatio} = \frac{\overrightarrow{I_{SpillNom}}}{\overrightarrow{I_{\mathrm{Re}\,fNom}}} \qquad \textbf{Eq. 2}$$

By re-arranging Eq. 1, and substituting for NomRatio and the latest value of $I_{Ref}$, the Expected Spill Current, $I_{Expected}$ can be calculated for any instant, as follows :-

$$\overrightarrow{I_{Expected}} = \overrightarrow{NomRatio} \times \overrightarrow{I_{\mathrm{Re}\,f}} \qquad \textbf{Eq. 3}$$

Using $I_{Expected}$ and $I_{Spill}$ (the measured spill current), $I_{Operate}$ is the difference between the two i.e.

$$\overrightarrow{I_{Operate}} = \overrightarrow{I_{Spill}} - \overrightarrow{I_{Expected}} \qquad \textbf{Eq. 4}$$

The RMS value of $I_{Operate}$ is calculated and compared with the Operate Setting.

## 3.2 Discussion of Principal of Operation and Measurement Accuracy

The choice of current transformer (CT) ratios is important to ensure optimum performance of the protection. CT ratio's for measurement of $I_{Ref}$ and $I_{Spill}$ should be chosen, so that at Nominal Operating Conditions i.e. Rated Voltage :-

$I_{Ref}$ Secondary $\geq$ $I_{Spill}$ Secondary

If through poor choice of CT ratio's and/or high standing spill current, $I_{Spill}$ Secondary > $I_{Ref}$ Secondary and therefore the settings entered for $I_{RefNom}$ and $I_{SpillNom}$ produce an NomRatio which is > 1, then the accuracy of the protection element will be impaired, since measurement errors inherent in $I_{Ref}$ are multiplied by NomRatio, see Eq. 3.

**For this reason, it is strongly recommended that CT ratio's are chosen to ensure that the ratio of $I_{SpillNom}$ to $I_{RefNom}$ is less than or equal to 1 i.e.**

$$\frac{\overrightarrow{I_{Spill}}}{\overrightarrow{I_{\mathrm{Re}\,f}}} \leq 1$$

If this is not the case then the accuracy and the minimum setting, which may be applied, will be degraded as follows :-

**Minimum Applied Setting** :-

Minimum Applied Setting ≥ $\left(5 \times \frac{\overrightarrow{I_{Spill}}}{\overrightarrow{I_{\mathrm{Re}\,f}}}\right) \times$ Minimum Relay Setting

or Minimum Relay Setting, whichever is greater.
**Eq. 5**

**Accuracy** :-

Accuracy ≤ $\left(5 \times \frac{\overrightarrow{I_{Spill}}}{\overrightarrow{I_{\mathrm{Re}\,f}}}\right)\%$ or 5% whichever is greater.

**Eq. 6**

Note :-

The above calculations for Minimum Applied Setting and Accuracy include a 5x safety margin.

**Consider this example :-**

The values entered for $I_{RefNom}$ and $I_{SpillNom}$ are such that $I_{SpillNom}$ is 4 x $I_{RefNom}$, and produce a NomRatio vector, which is the equivalent of 4x.

Therefore the Minimum Setting which may be applied is (see Eq. 5) :-

(5 x 4) x 0.02 x In = **0.40 x In**

And the Accuracy will be degraded to (see Eq. 6) :-

(5 x 4)% = **20%**

## 3.3 Application of the Capacitor Unbalance Element

During the construction of the capacitor bank, it is common practice to measure the capacitance of each element of the making up the capacitor bank and then calculate the expected standing spill, for each phase.

The capacitor bank will be energised and the standing spill for each phase measured and checked against the calculated value.

After de-energisation, the capacitance of each element will then be measured again, to confirm that there are no failures following initial energisation.

The standing spill correction settings, are calculated and checked during testing, as described above. The Reference currents would normally be set to the default value of 1.00 xIn and the Spill current magnitude setting would be the calculated spill for each phase capacitor configuration.

In the case of capacitor bank shown in Figure 5 – Capacitor Unbalance - Single Phase Bridge Connection Schematic, the spill current of capacitor C1 and capacitor C2 will be normally be in-phase or in anti-phase to the reference current, therefore the angle setting for the spill current any particular phase would be 0˚ or 180˚. The relay includes, the setting range –180˚ to 180˚ in 1˚ steps, to cater for situations where the Spill Angle may not be exactly 0˚ or 180˚, or the capacitor configuration is such that the nominal angles are not 0˚ and 180˚.

The Cx 50-1 element setting would be calculated based on the number of fuse failures required to generate an alarm condition. For example, a single fuse failure, the setting would be 20-80% of the spill current due to the failure and for a failure of two fuses the setting may be 75% of the calculated current, so that the alarm will not operate for a failure of one fuse, but is sure to operate for failure of two fuses.

The Cx 50-2 element would normally be used as the trip element and the setting calculation would be based on the number of fuse failures, which would be deemed a fault condition, the general formula would be :-

$$Setting = \frac{\left((N-1) + {}^{P}\!/_{100}\right) * Spill}{N}$$

where :

N = Number of fuse failures.

P = Percentage of single fuse failure for stability.

Spill = Calculated spill current for failure of N fuses.

# 4 PHASE UNBALANCE PROTECTION

The Phase Unbalance element calculates the RMS phase residual current, which is then applied to an overcurrent detector, with a following DTL. This element will primarily be applied as a backup protection, which will detect open circuit faults on one or two capacitor bank phases.

Consider Figure 6 – Phase Unbalance – Backup Open Circuit Protection, which shows the protective zone for open circuits, an open circuit, within this zone, in any single or two phases,will cause an increase in residual current. The setting must be chosen to provide adequate operation at the minimum generated residual current for single or two phase open-circuits, as a guide 20% of rated capacitor bank current is a common setting.

# 5 CURRENT TRANSFORMER REQUIREMENTS

The current transformer requirements are dominated by the requirements for the Overall Differential protection – please refer to the current transformer requirements for that particular protection element, when determining the CT requirements.

# 6 DIAGRAMS

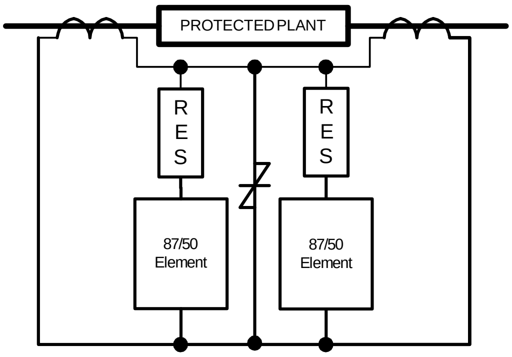

Figure 1 – Basic Dual Element High Impedance Differential Protection

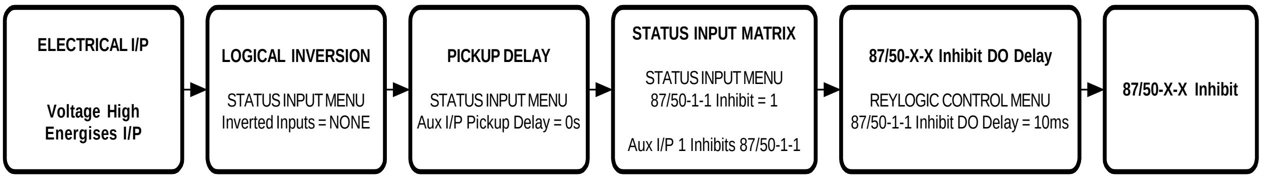

Figure 2 – Application of 87/50 Inhibit DO Delay

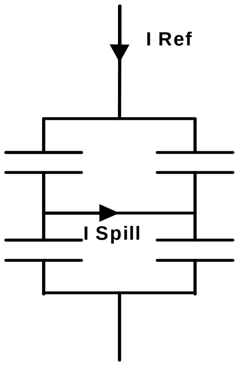

Figure 3 - Simplified Single Phase Bridge Capacitor Bank

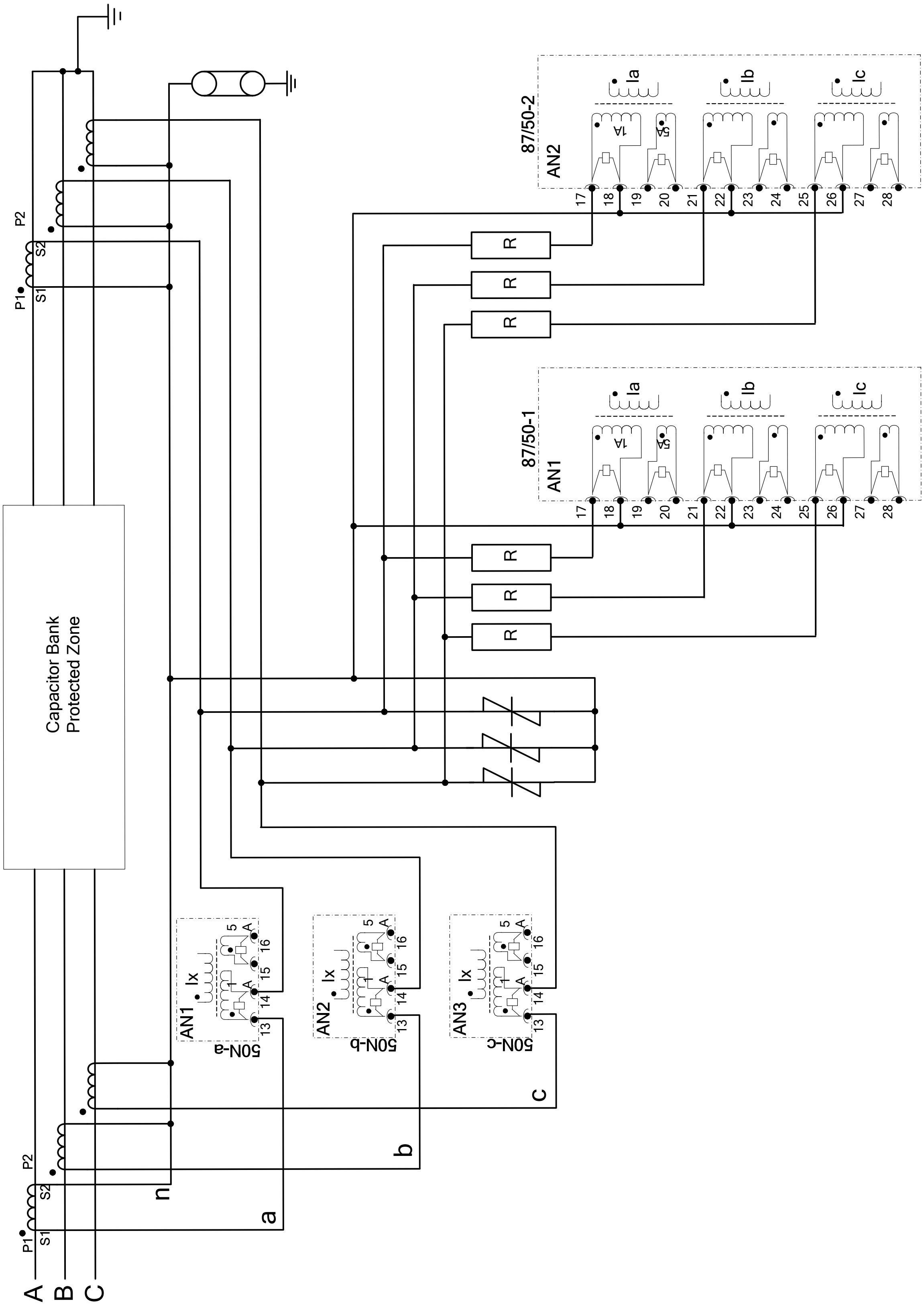

**Figure 4 – Typical Dual High Impedance scheme with additional 50N protection**

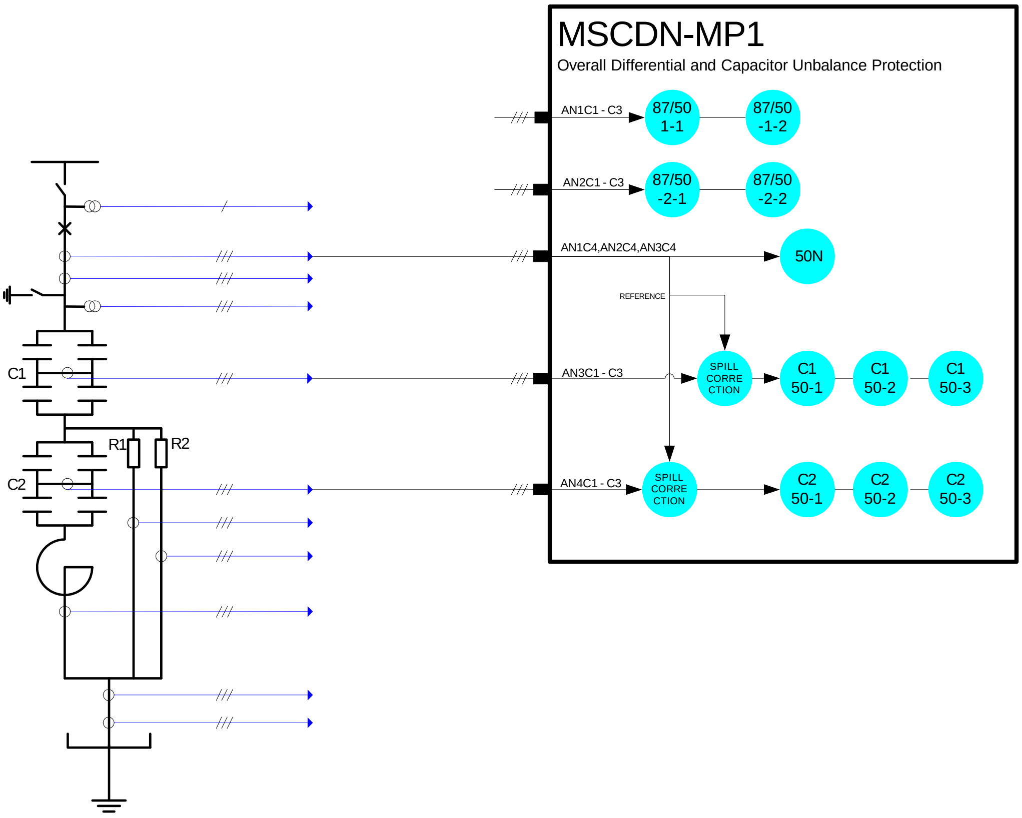

Figure 5 – Capacitor Unbalance - Single Phase Bridge Connection Schematic

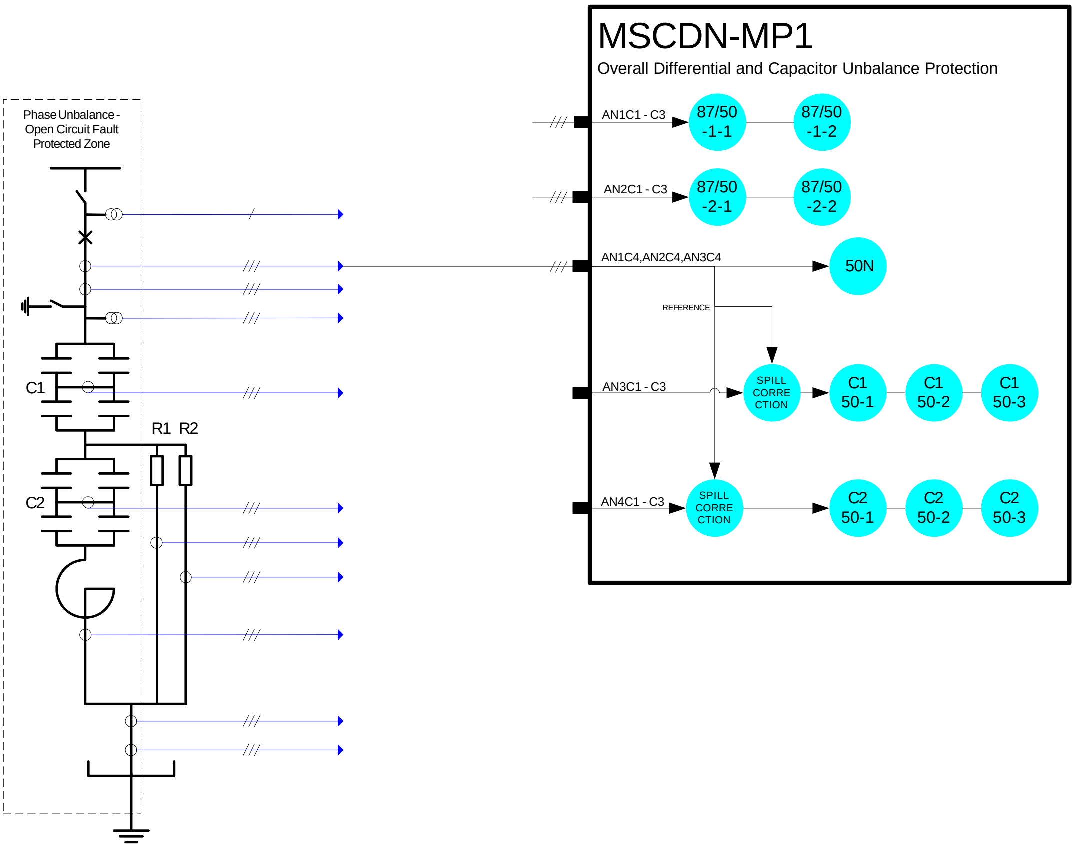

Figure 6 – Phase Unbalance – Backup Open Circuit Protection